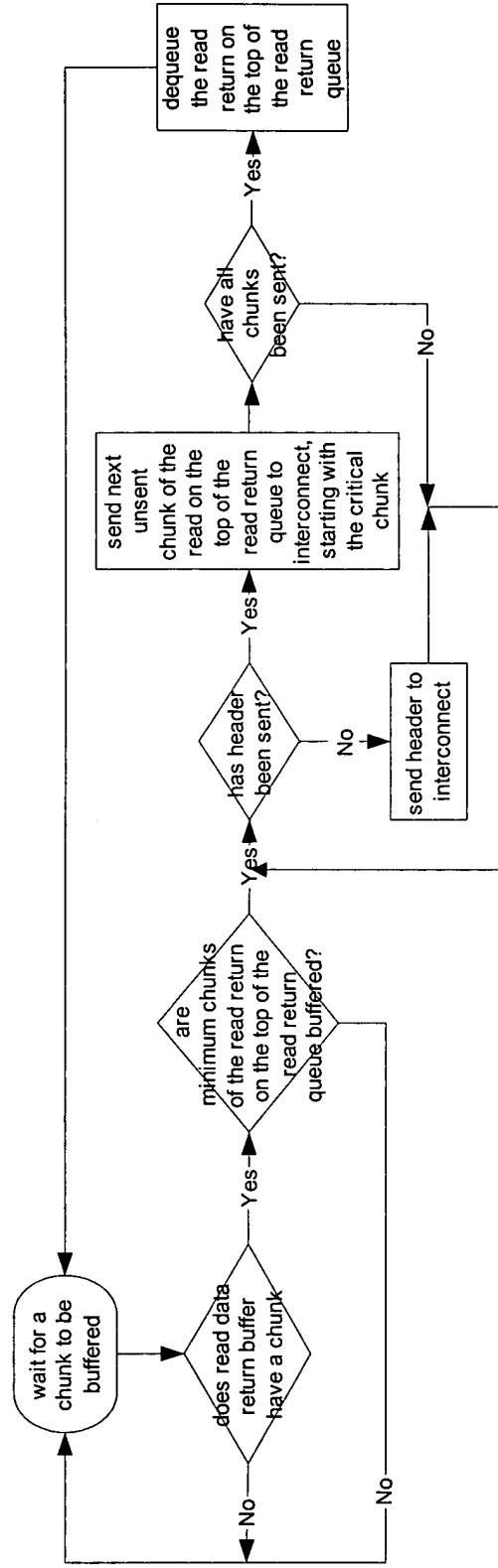


Decision in the figure may be done every flit clock cycle



Store and forward data return  
Figure 1A (Prior Art)

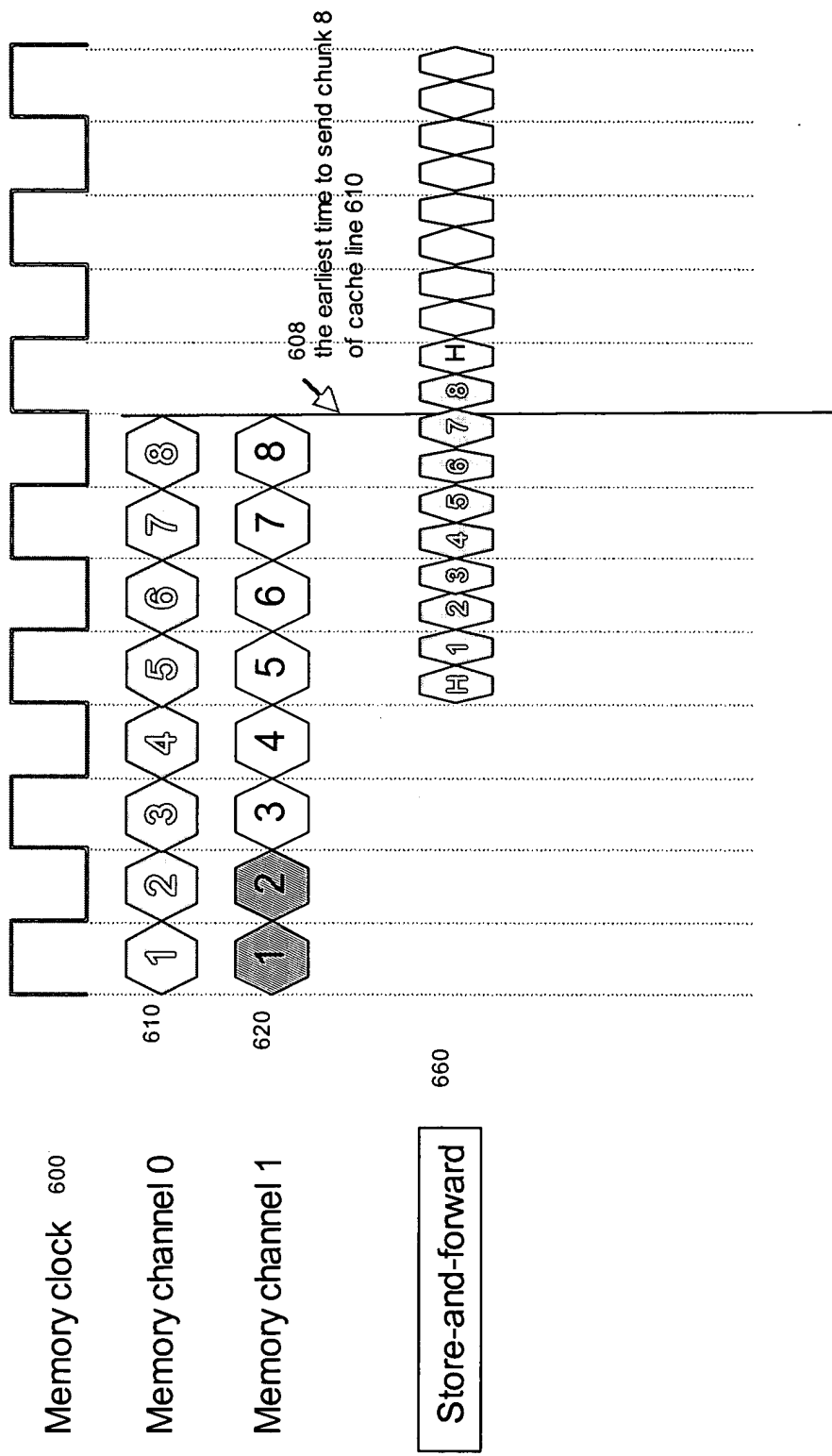


Figure 1B

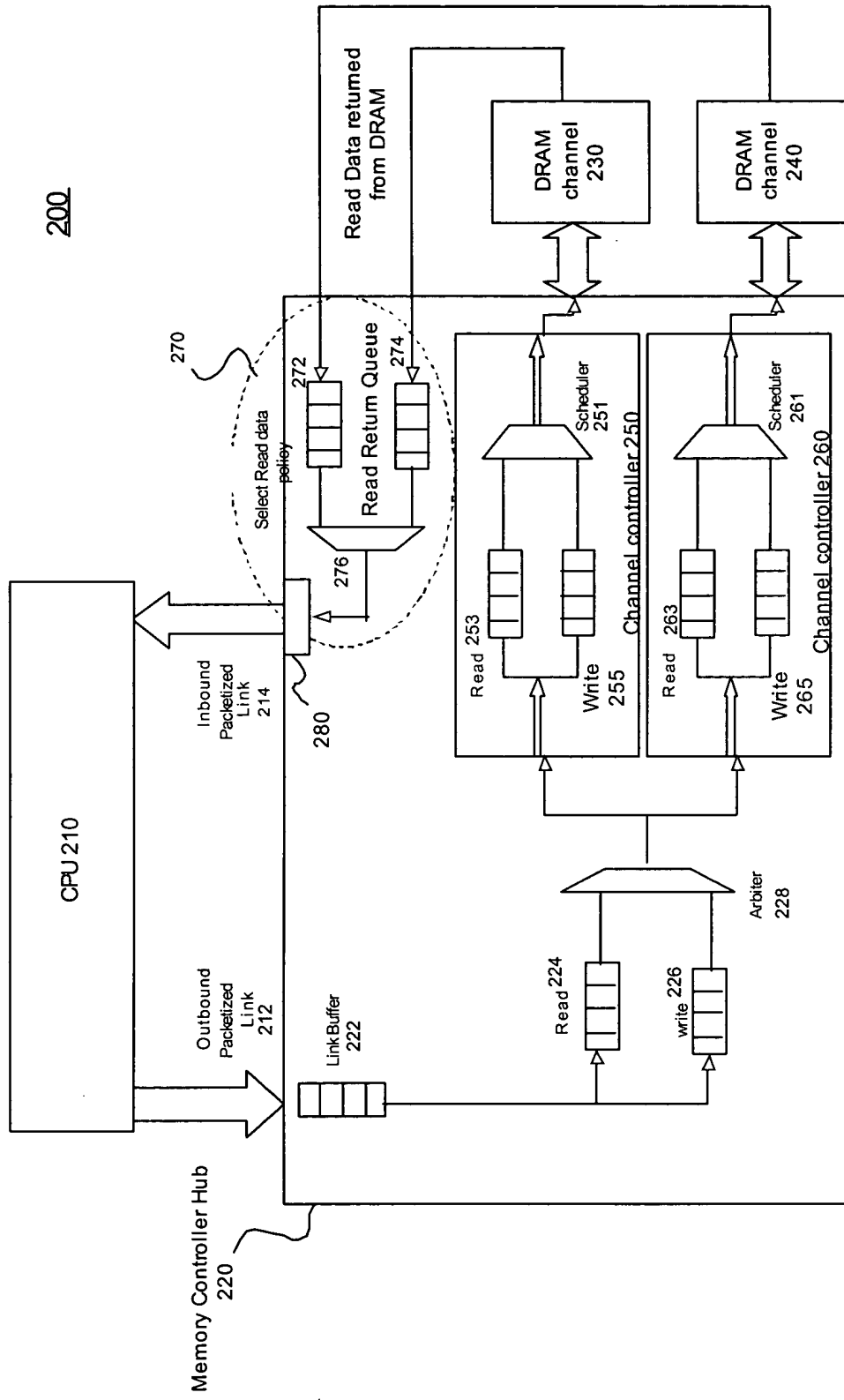
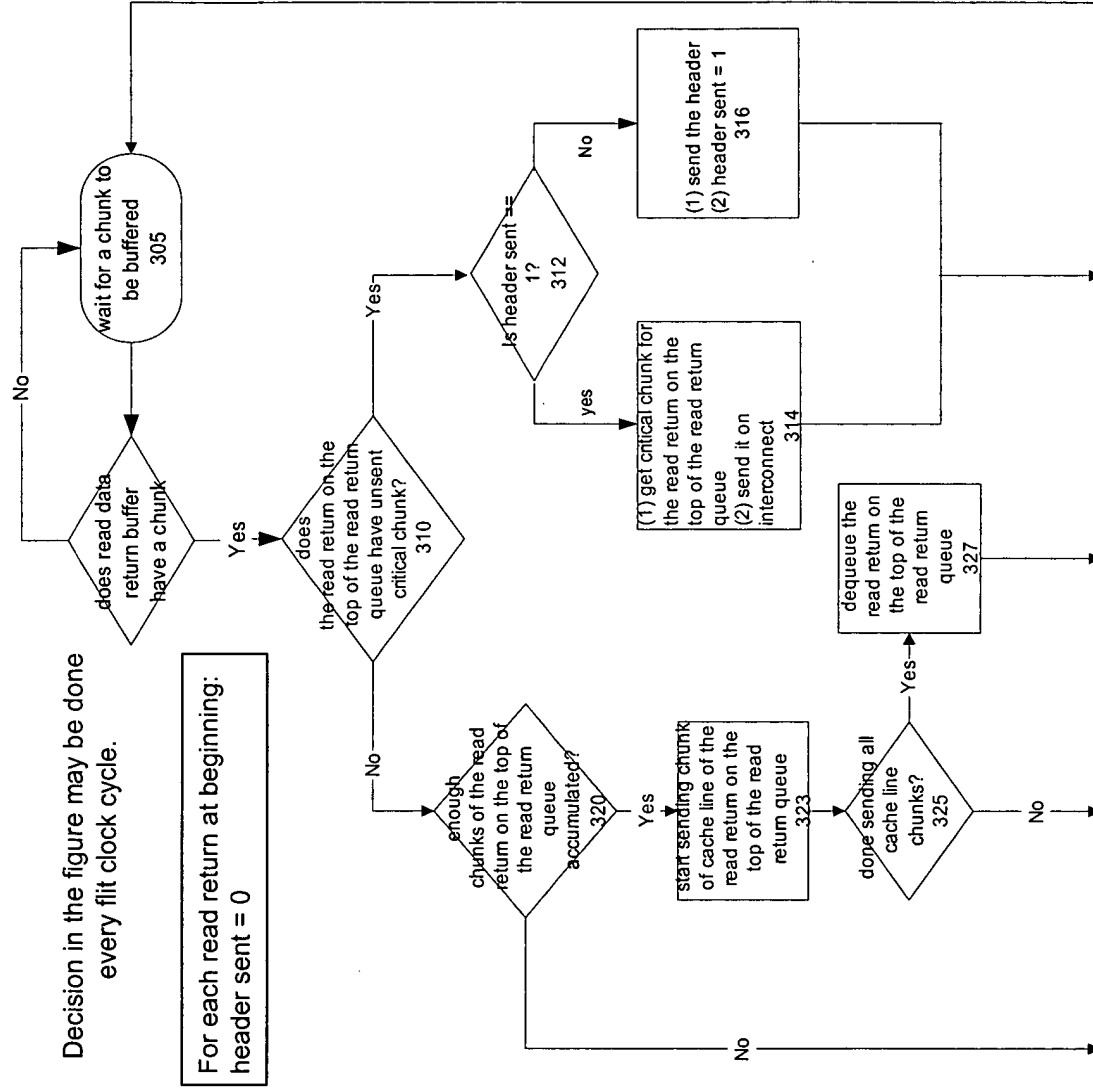


Figure 2



Critical chunk with bubble  
Figure 3A

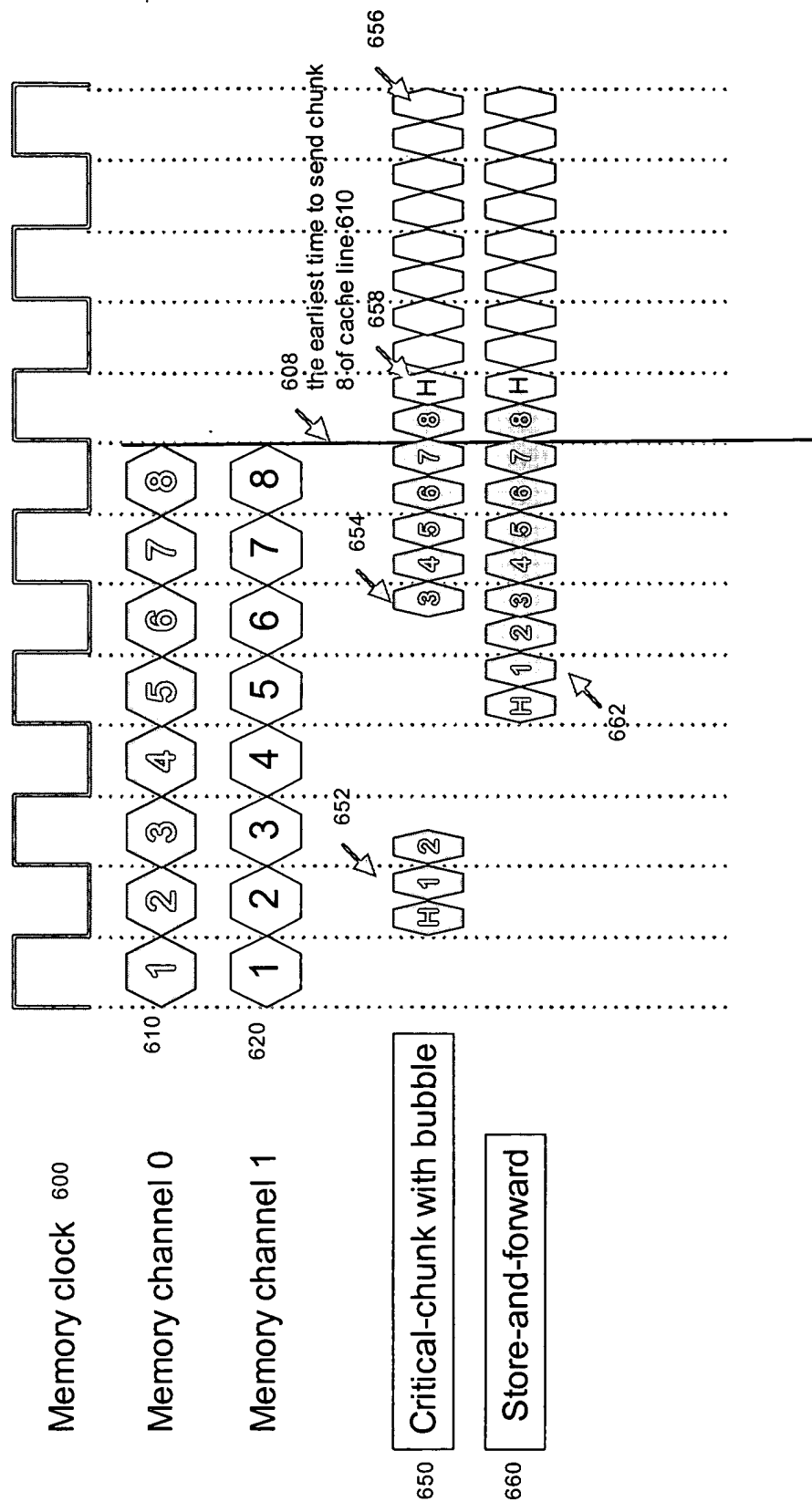
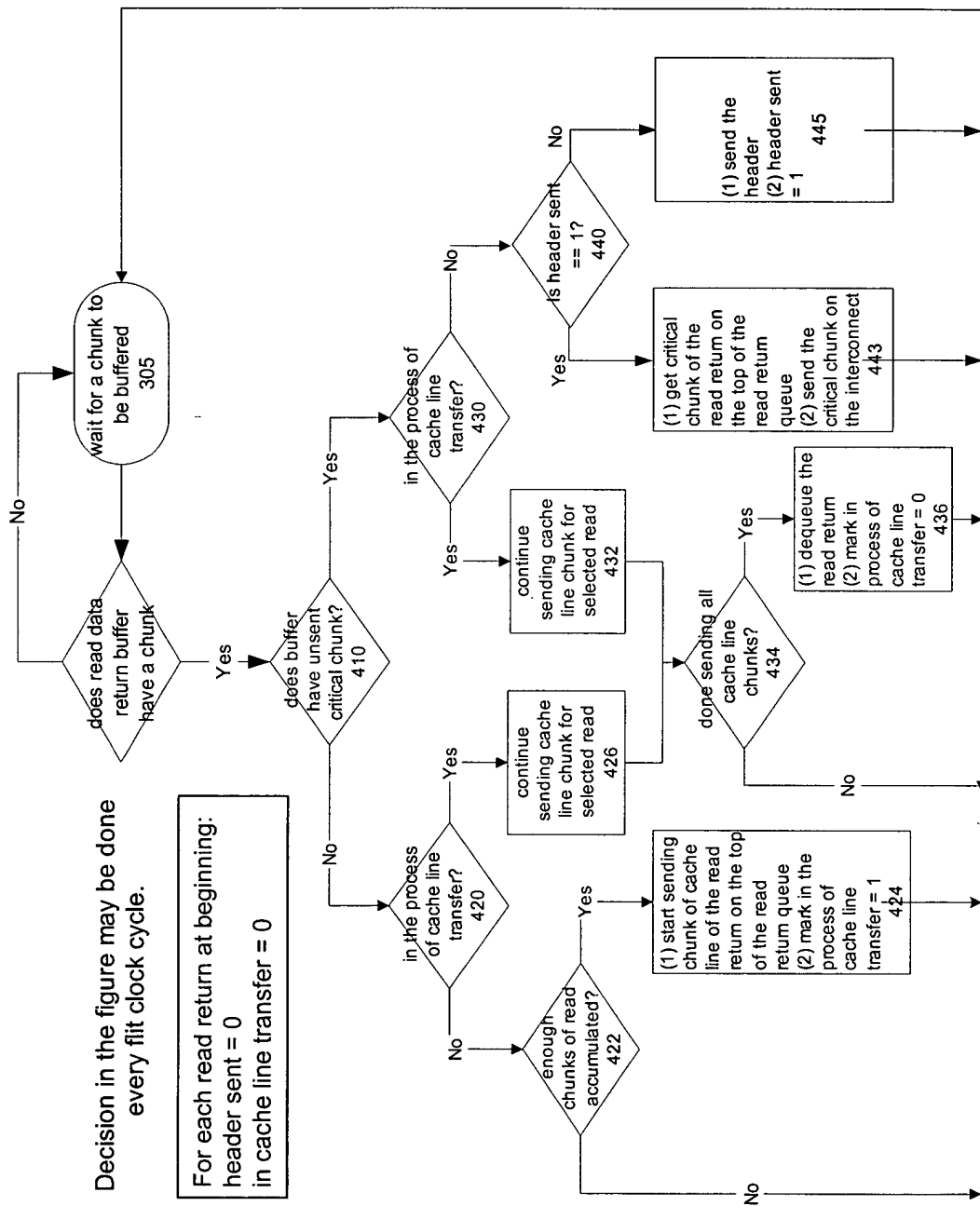


Figure 3B



Critical chunk interleaved read return  
Figure 4A

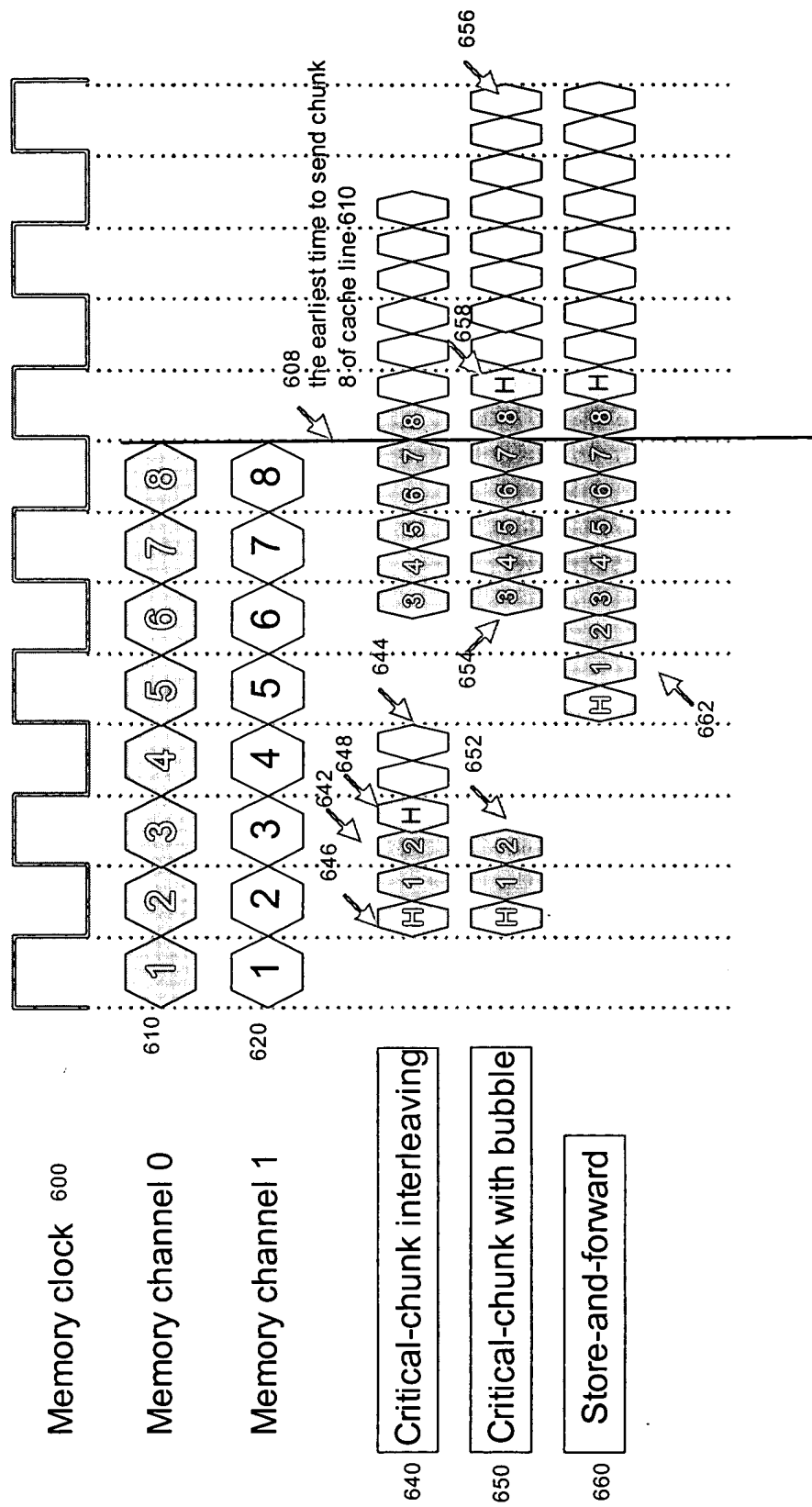
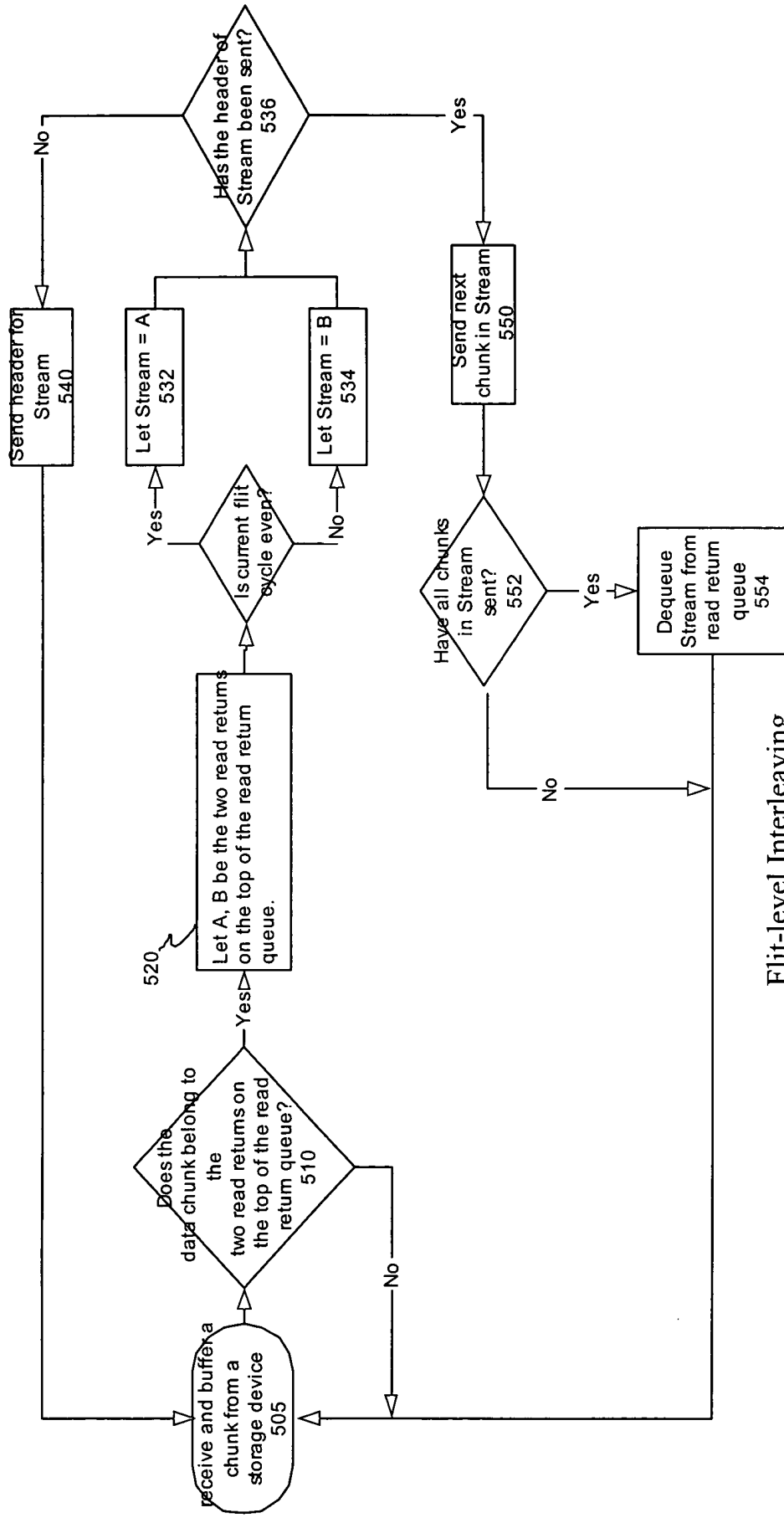


Figure 4B

Decision in the Figure may be done every flit clock cycle.



Flit-level Interleaving  
Figure 5A



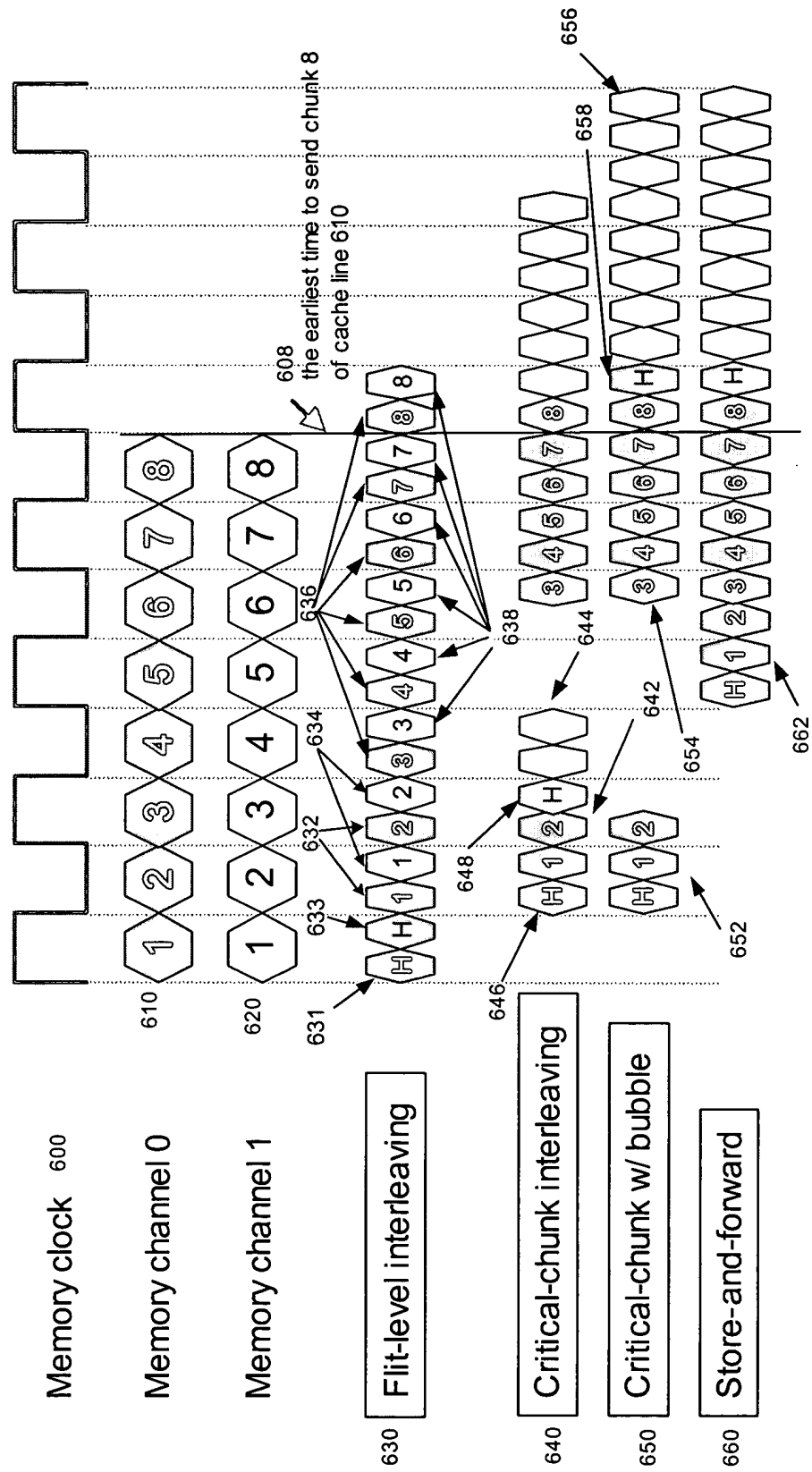


Figure 5B



Figure 5C

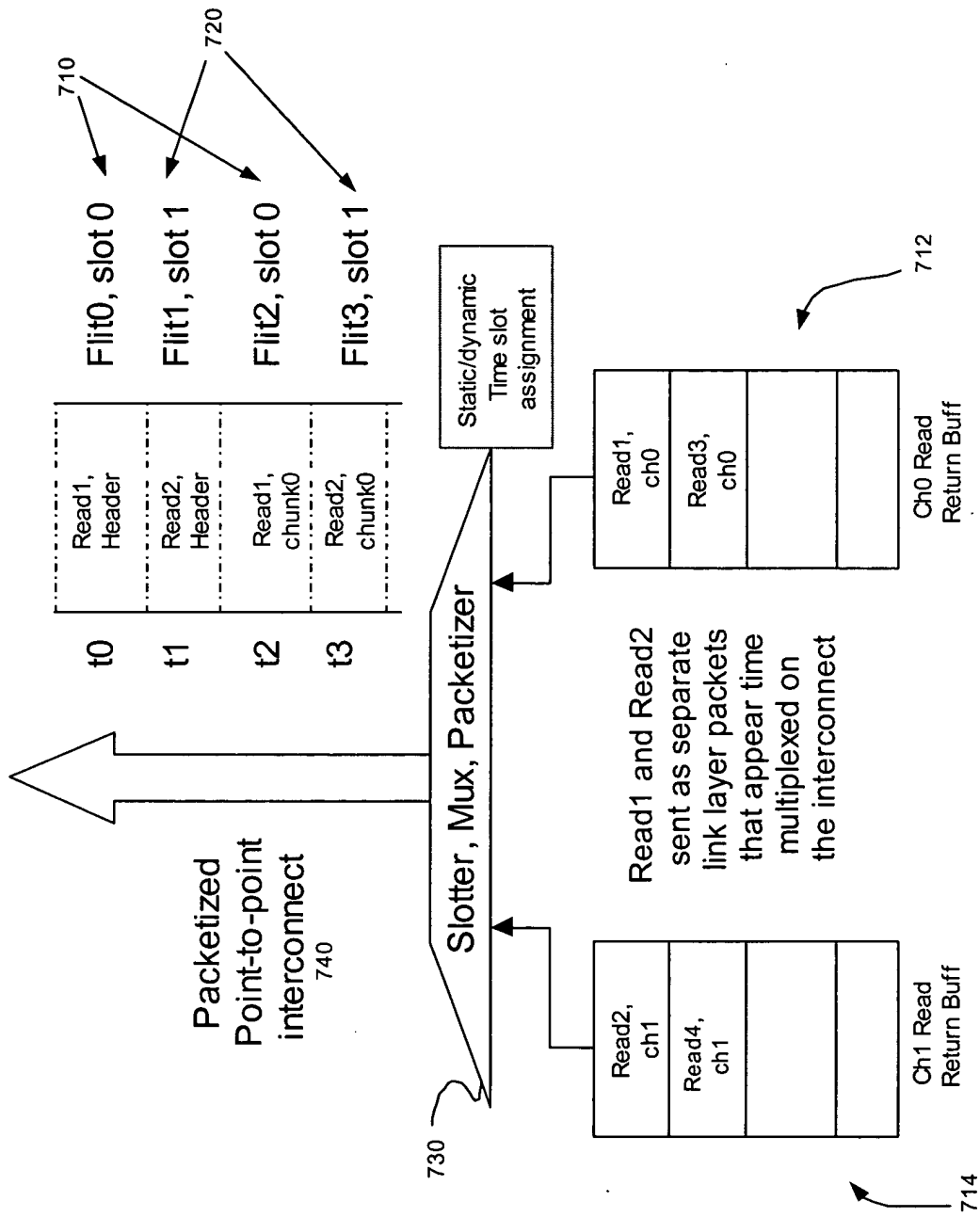


Figure 6A

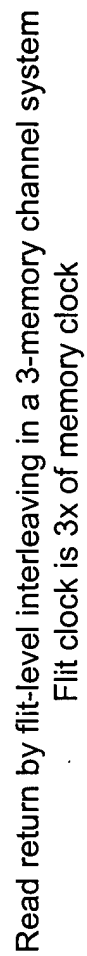
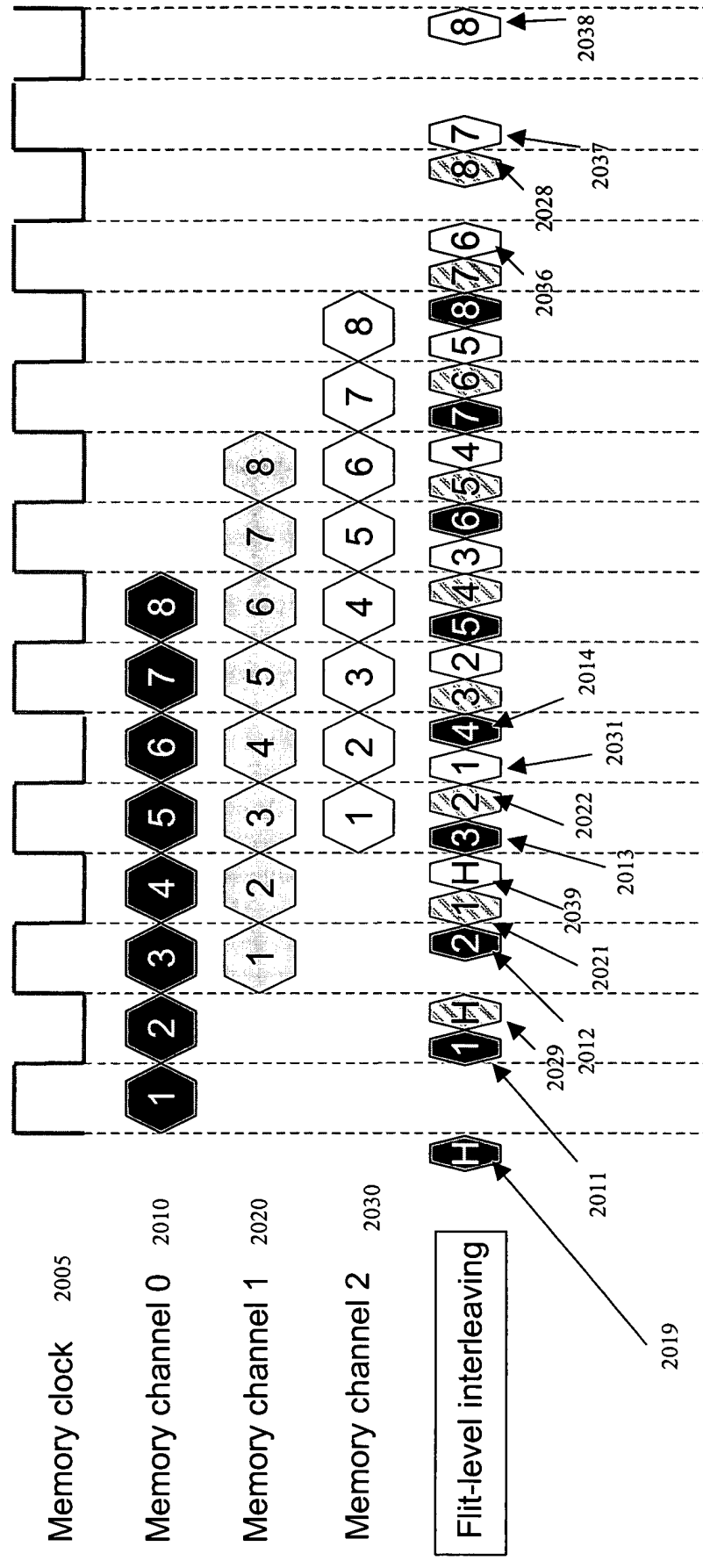
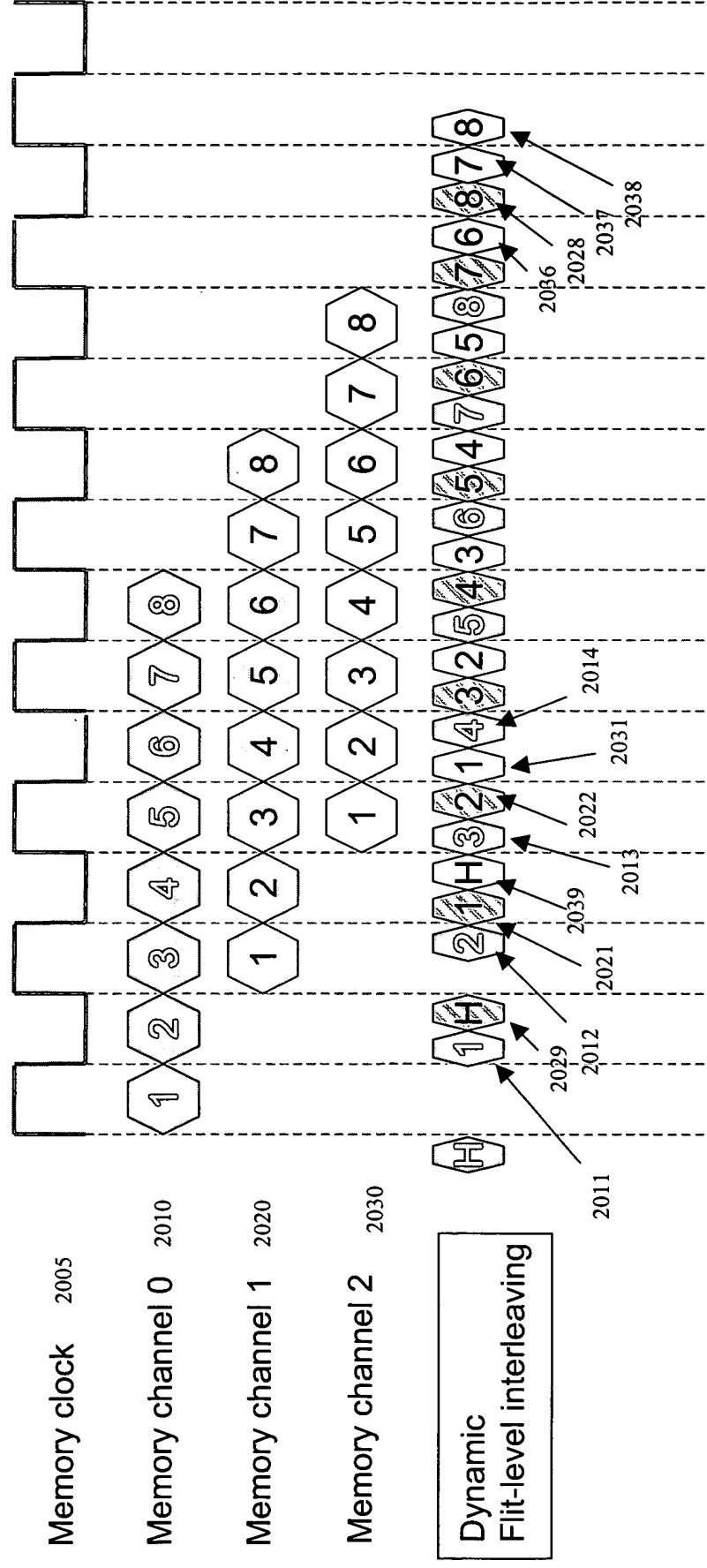


Figure 6B



Read return by flit-level interleaving in a 3-memory channel system  
 Flit clock is 2x of memory clock

Figure 6C



Read return by flit-level interleaving in a 3-memory channel system  
 Flit clock is 2x of memory clock

Figure 6D